

001230" 5424960

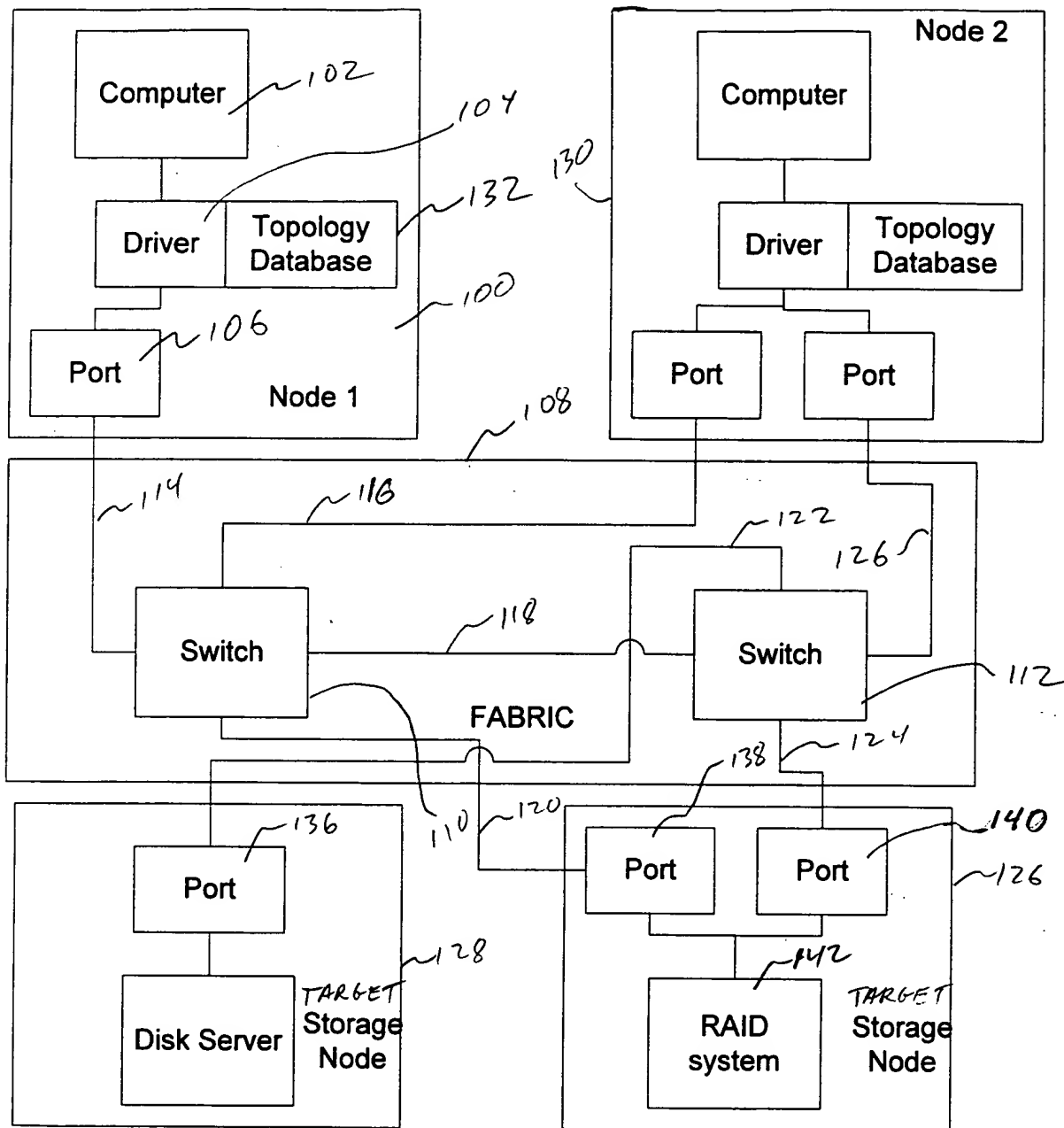


Figure 1

007220" 3454960

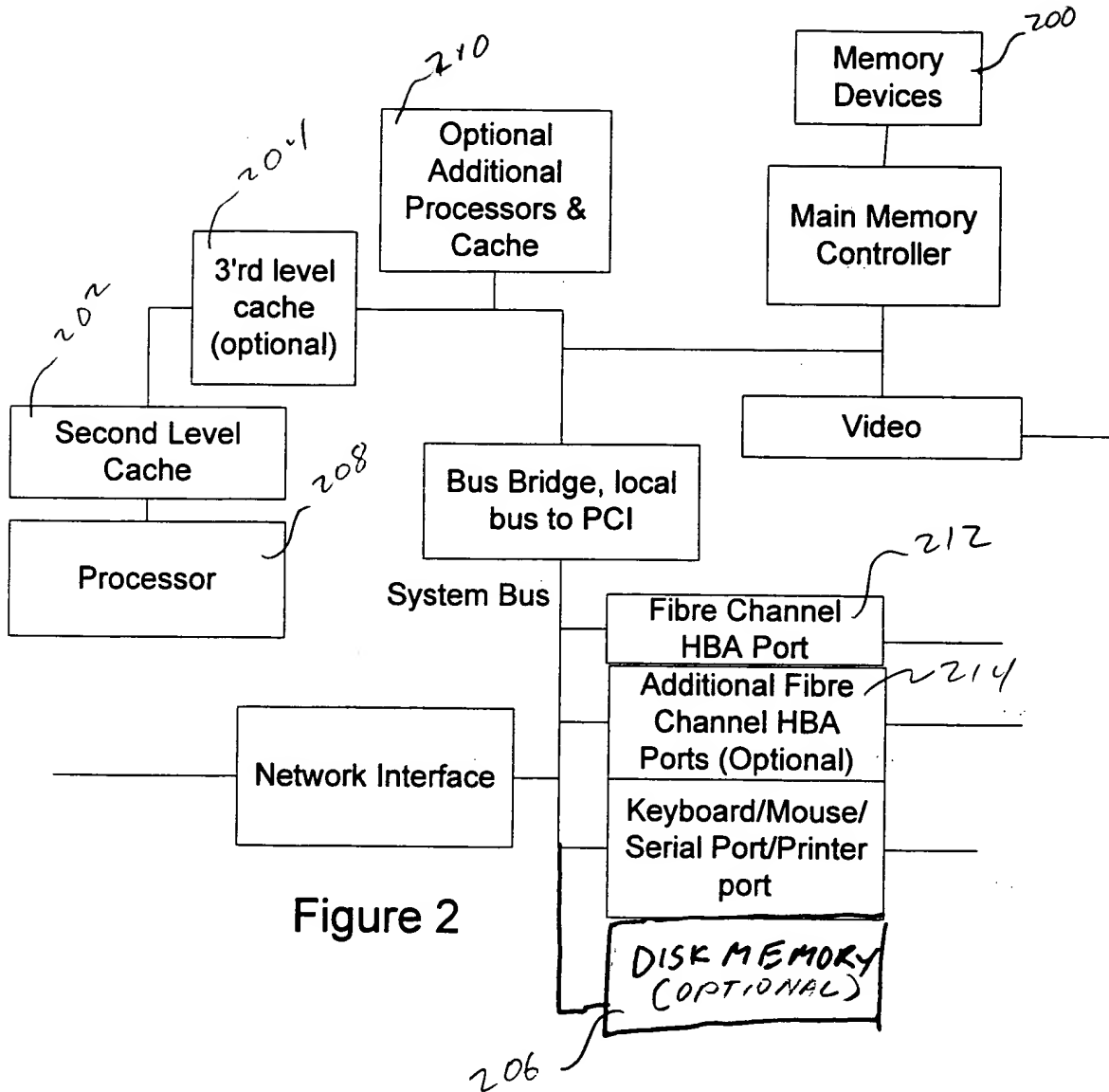


Figure 2

007280" 52524960

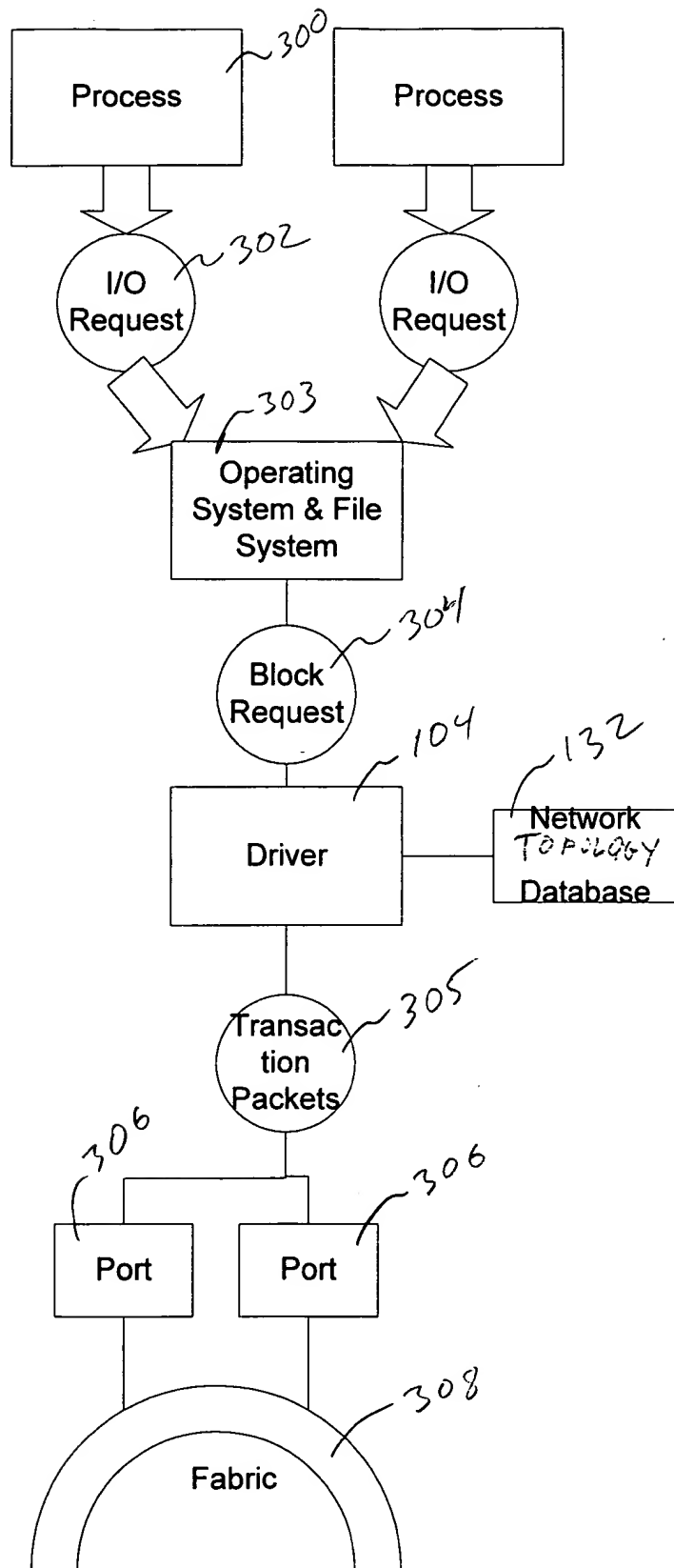


Figure 3

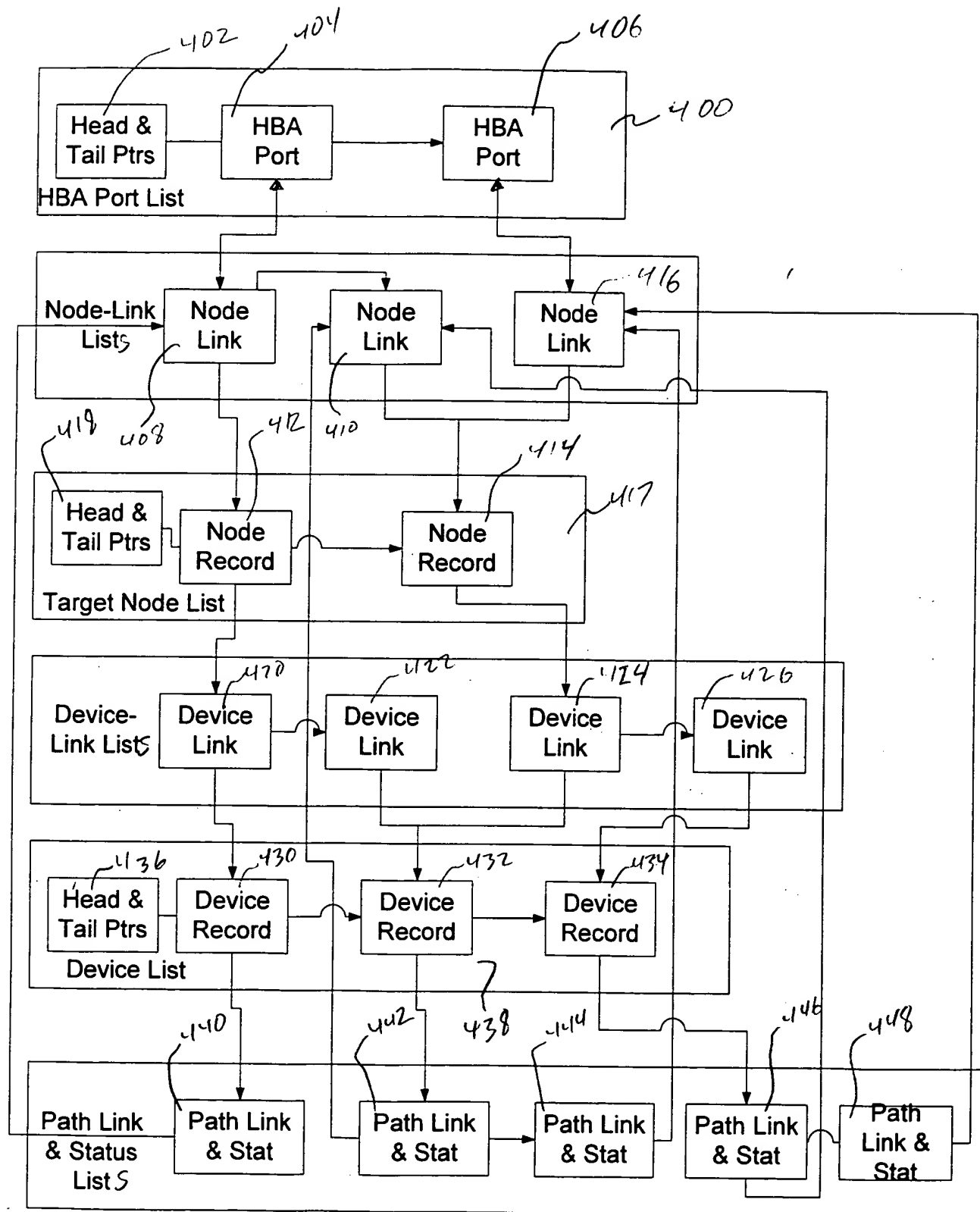
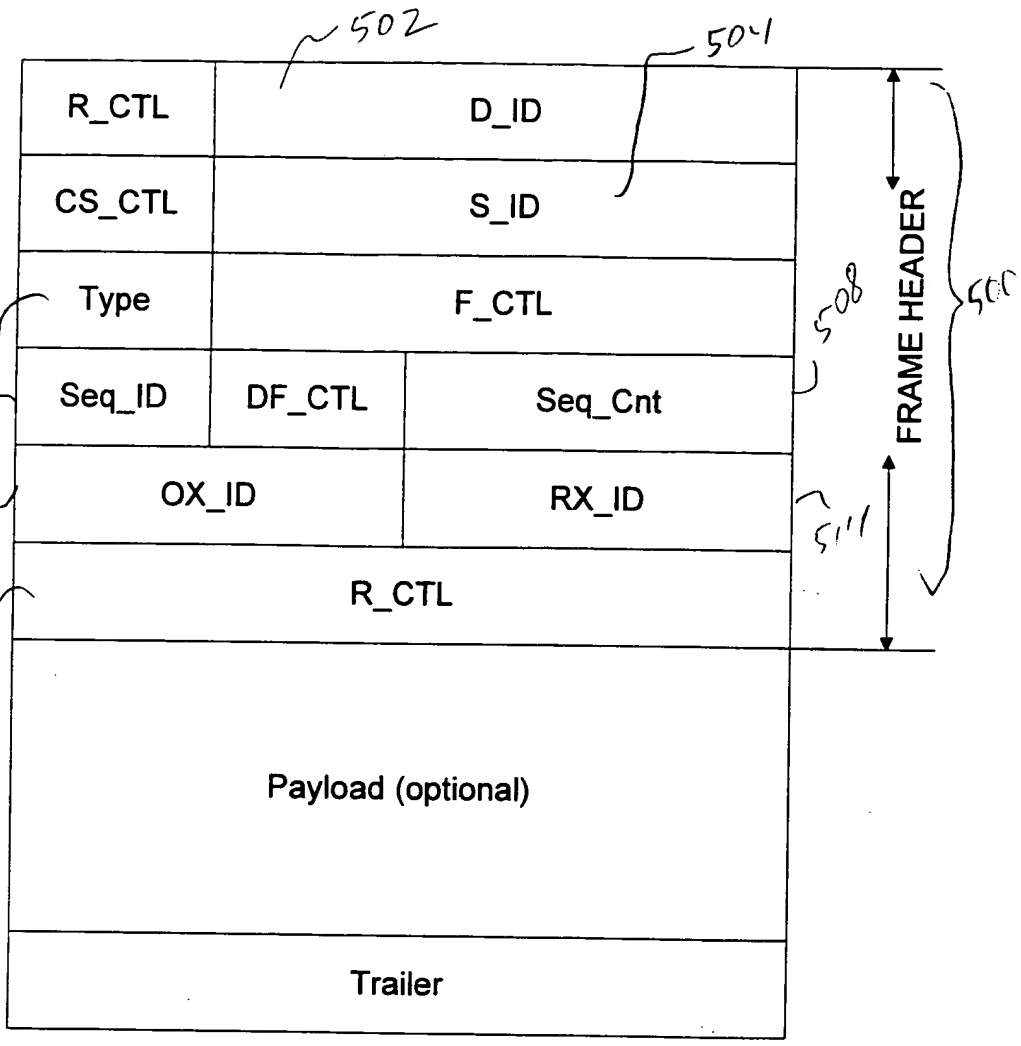


Figure 4

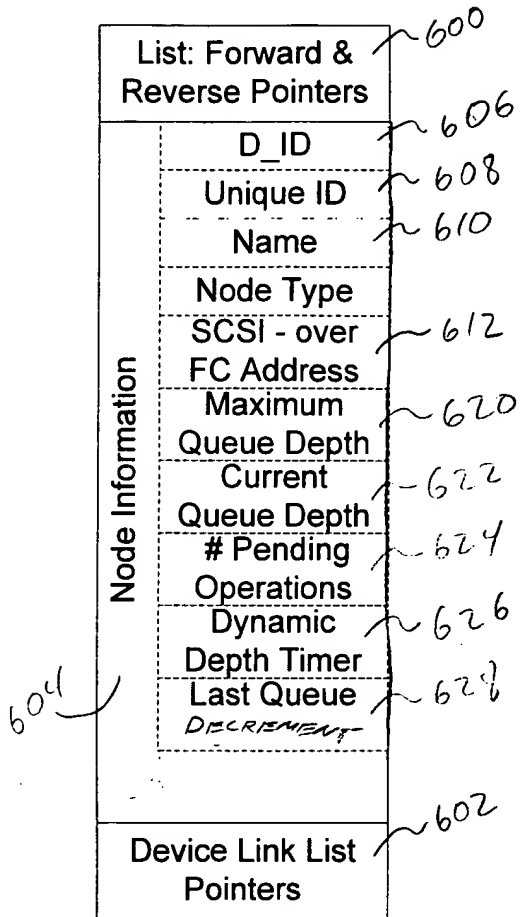
00T280" 52524960



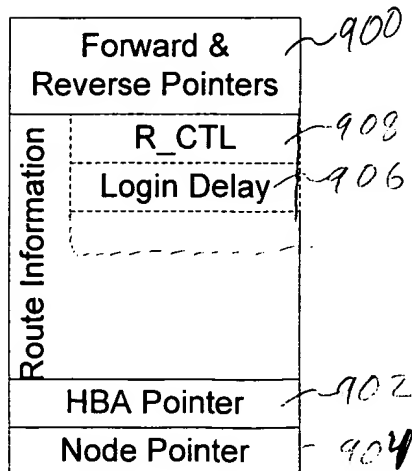
Frame Structure

KNOWN ART

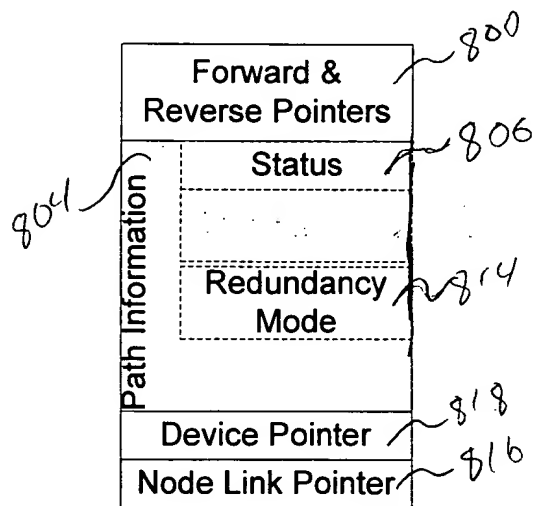
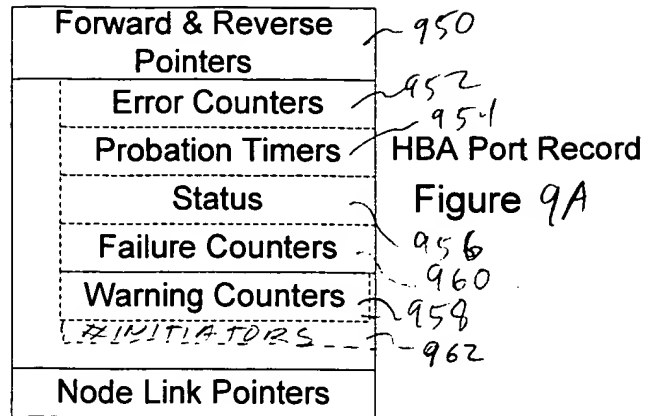
Figure 5



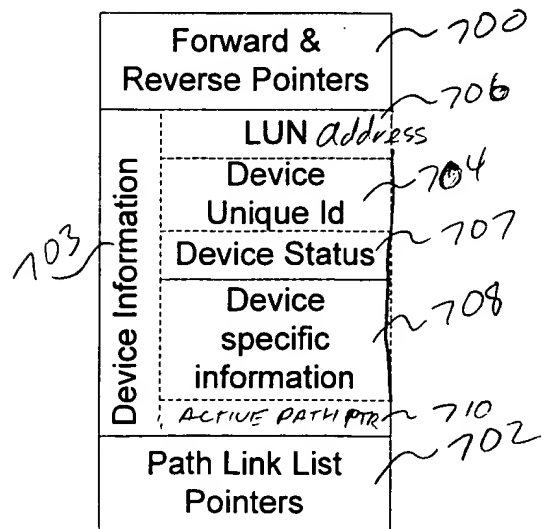
Node Record Figure 6



Node Link Figure 9



Path Link Figure 8



Device Record

Figure 7

09642575-082100

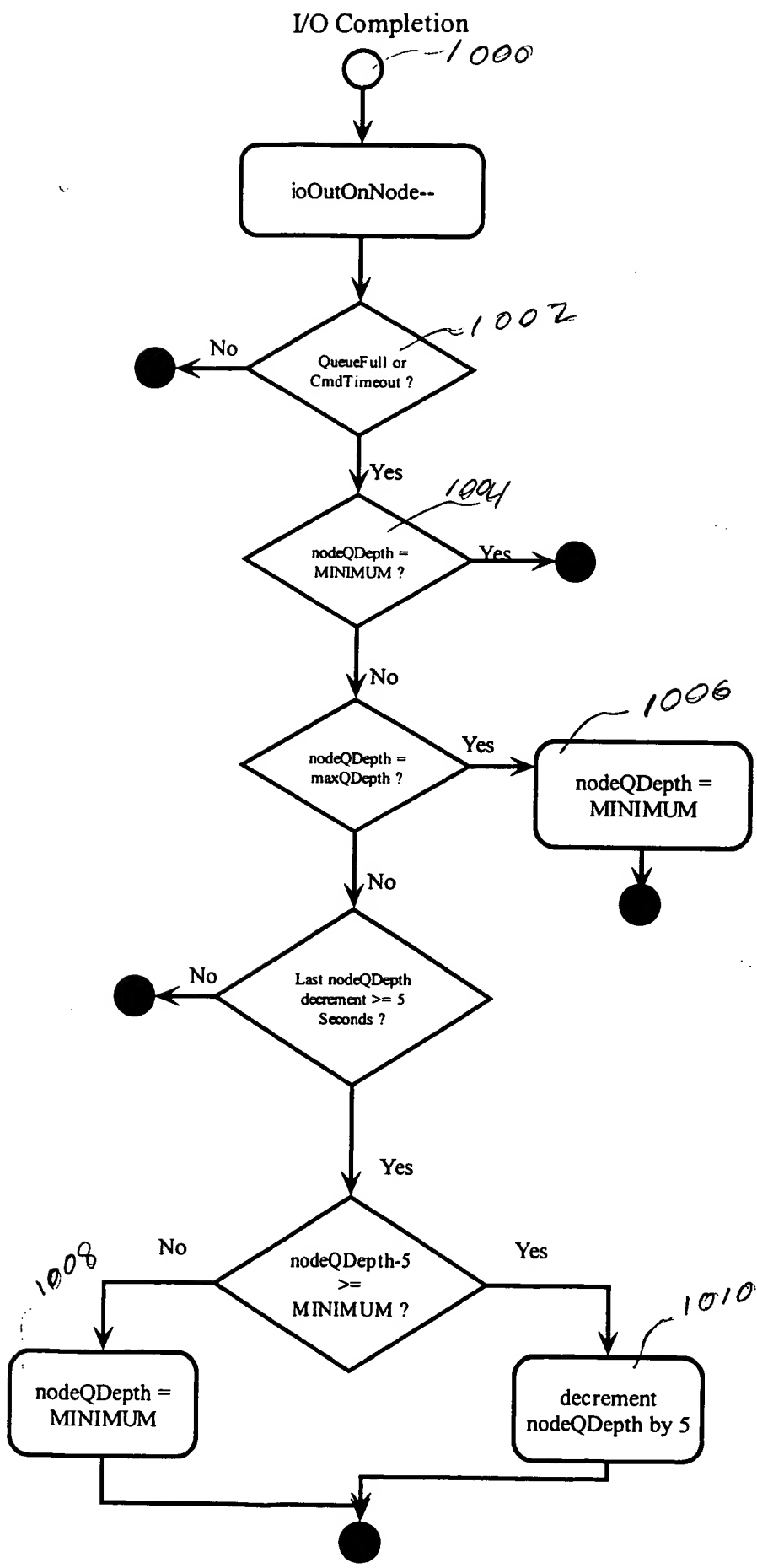


Figure 10

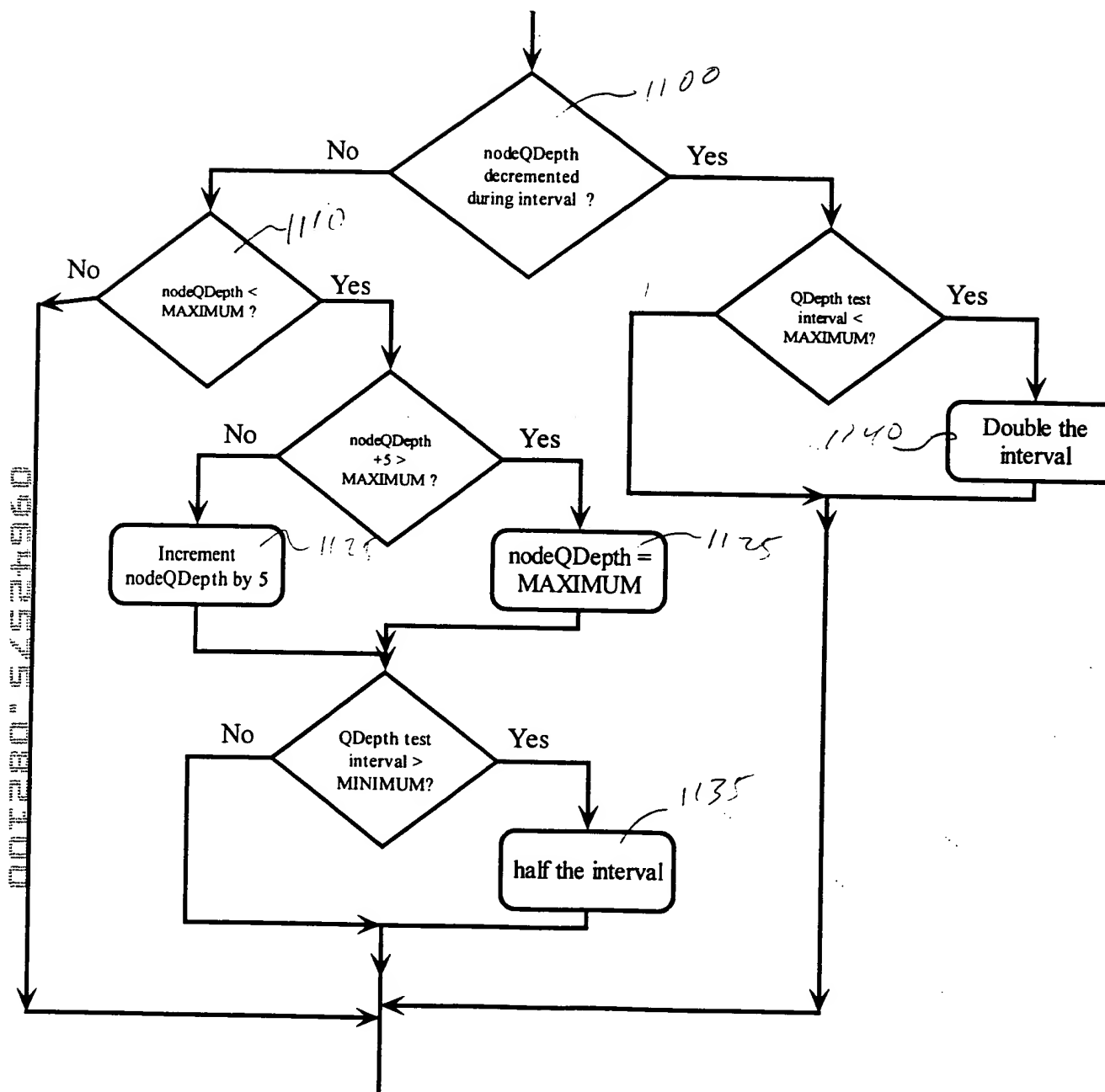


Figure 11



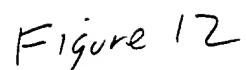
[illegible]

Figure 12

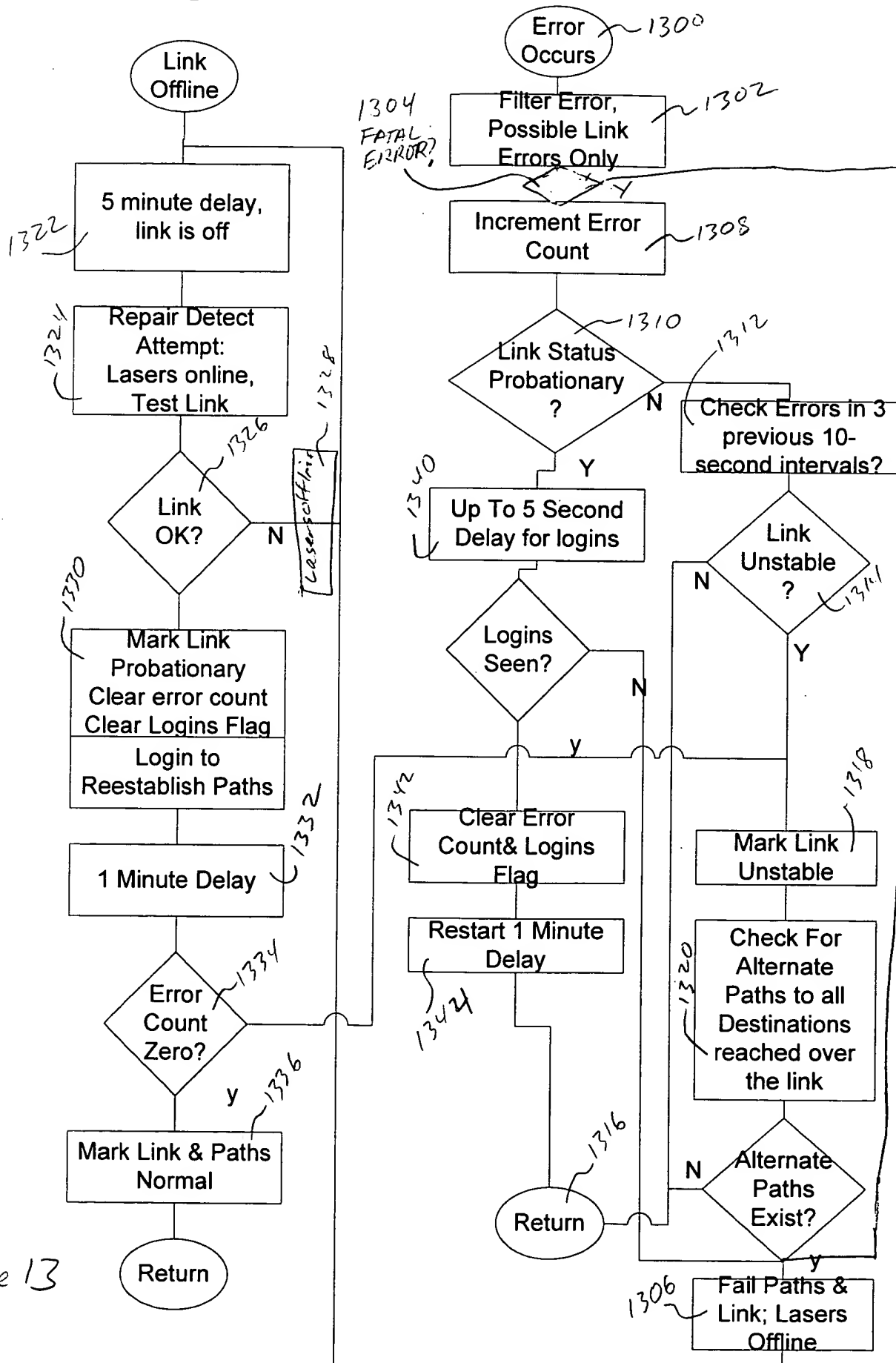


Figure 13

REPAIR  
Detected

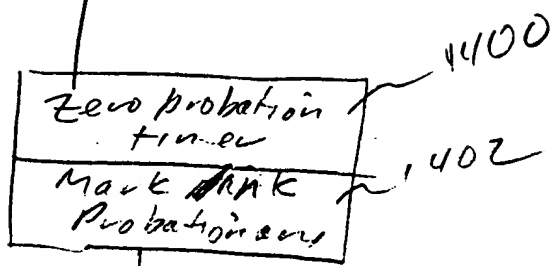


Figure 14

001230" 54524960

```

graph TD
    Start([Exchange Start]) --> D1{active path pin valid?}
    D1 -- Y --> P1[ ]
    D1 -- N --> D2{path active?}
    D2 -- Y --> P1
    D2 -- N --> D3{path normal?}
    D3 -- Y --> P1
    D3 -- N --> D4{path probationary?}
    D4 -- Y --> P2[ ]
    D4 -- N --> D5{was any path taken off line as unstable or failed?}
    P1 --> P1_1[ ]
    P1_1 --> P1_2[ ]
    P1_2 --> P1_3[ ]
    P1_3 --> P1_4[ ]
    P1_4 --> P1_5[ ]
    P1_5 --> P1_6[ ]
    P1_6 --> P1_7[ ]
    P1_7 --> P1_8[ ]
    P1_8 --> P1_9[ ]
    P1_9 --> P1_10[ ]
    P1_10 --> P1_11[ ]
    P1_11 --> P1_12[ ]
    P1_12 --> P1_13[ ]
    P1_13 --> P1_14[ ]
    P1_14 --> P1_15[ ]
    P1_15 --> P1_16[ ]
    P1_16 --> P1_17[ ]
    P1_17 --> P1_18[ ]
    P1_18 --> P1_19[ ]
    P1_19 --> P1_20[ ]
    P1_20 --> P1_21[ ]
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    P1_22 --> P1_23[ ]
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    P1_27 --> P1_28[ ]
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    P1_29 --> P1_30[ ]
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Figure 15